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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

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SANJAY MEHROTRA

Serial No.: 09/310,880

Filed: May 14, 1999

For: FLASH EEPROM SYSTEM

Group Art Unit: 2818

San Francisco, California

Assistant Commissioner of Patents
Washington, D.C. 20231

SECOND PRELIMINARY AMENDMENT

Sir:

Please add the following new claims to the above-referenced patent application:

14 ~~-26.~~ A memory comprising:

an array cell having an output, an array threshold value set to one of n array threshold values to control a signal provided at the array cell output, and a gate;

a reference cell having an output, a floating gate which stores an electrical charge to allow a reference threshold value to be programmed, and a gate, the reference cell having its reference threshold value programmed between two successive ones of the n array threshold values to control a signal provided at the reference cell output;

a comparison circuit coupled to the array cell output and the reference cell output, the comparison circuit for comparing the signal at the array cell output to the signal at the reference cell output and providing a signal indicating which of the n array threshold values is held by the array cell; and

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a power supply for supplying a supply voltage to the gate of the array cell to enable the array cell to provide the signal at the array cell output, the power supply further supplying the supply voltage to the gate of the programmable reference cell to enable the reference cell to provide the signal at the reference cell output.

15 ~~77.~~ The memory of claim ~~76~~ 14 wherein when a value of the supply voltage is varied, a working margin between the array cell output and the reference cell output remains constant.

16 ~~78.~~ The memory of claim ~~76~~ 14 wherein n is greater than two.

17 ~~79.~~ A memory comprising:

a first word line;

a second word line;

a power supply for providing a substantially identical supply voltage to the first word line and the second word line;

an array cell having a gate connected to the first word line and a source-to-drain path, the array cell having a threshold value set to one of n array threshold values;

n-1 read reference cells, each read reference cell having a gate connected to the second word line, a source-to-drain path and a floating gate which stores an electrical charge to allow a reference threshold value to be programmed, each respective read reference cell having its reference threshold value programmed between two different successive ones of the n array threshold values; and

read sense amplifiers, each read sense amplifier having a first input coupled to the source-to-drain path of the array cell and a second input coupled to the source-to-drain path of a respective one of the read reference cells, each read sense amplifier for providing an output signal indicating whether a signal received at its first input is greater than a signal received at its second input.

18 ~~80.~~ The memory of claim ~~79~~ 17 wherein n is greater than two.--

REMARKS

Claims 76-78 are exact copies of respective claims 1-3 of U.S. patent no. 5,828,601 - Hollmer et al., granted October 27, 1998. Claims 79 and 80 are exact copies of respective Hollmer